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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/680,665	10/06/2003	George Matamis	SNDK.294US0	5425

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EXAMINER	
DOTY, HEATHER ANNE	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 06/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/680,665	MATAMIS ET AL.	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,8-18,20-31 and 33-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-5,8-18,20-26,31 and 33-36* is/are allowed.

6)☒ Claim(s) *27-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Duuren et al. (U.S. 2005/0218445) in view of Joo et al. (U.S. 6,204,122).

Regarding claim 27, Van Duuren et al. teaches a method of making a non-volatile memory array, comprising a plurality of floating gates (**14** in Fig. 10) and forming a plurality of control gates (**18** in Fig. 10; paragraph 0039 specifies that the elements are plural) extending in a first direction and overlying the plurality of floating gates; forming insulating elements along sides of the plurality of floating gates that extend in the first direction (**22** in Fig. 5; paragraph 0051), the insulating elements extending above lower surfaces of the plurality of control gates (Fig. 5); and forming conductive sidewall portions overlying insulating elements (**24** in Fig. 10), the conductive portions in contact with control gates, but insulated from floating gates by the insulating elements (Fig. 9; paragraph 0061).

Van Duuren et al. does not expressly teach forming a plurality of strings of memory cells having strings of floating gates extending in a direction perpendicular to the direction of the plurality of control gates.

However, Joo et al. teaches that a conventional EEPROM (column 1, lines 13-67) comprises strings of memory cells having strings of floating gates (P2 in Fig. 2B) and perpendicular control gates (P3 in Fig. 2B—for orientation, compare Figs. 1A and 3 of the instant application to Joo et al.'s Figs. 2B and 1B, respectively).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Van Duuren et al., and further form the device to be a string of memory cells having strings of floating gates extending in a direction perpendicular to the direction of the plurality of control gates, since Joo et al. teaches that this is a conventional form for a function EEPROM.

Regarding claim 28, Van Duuren et al. and Joo et al. together teach the method of claim 27. Van Duurren et al. further teaches that the insulating elements are first formed to extend along the sides of the plurality of the floating gates and along sides of the plurality of control gates and are subsequently etched to provide a contact area to the control gates (paragraph 0050).

Regarding claim 29, Van Duuren et al. and Joo et al. together teach the method of claim 27. Van Duuren et al. further teaches, subsequent to the forming the conductive sidewall portions, implanting source and drain regions (**20** in Fig. 8; paragraph 0048).

Regarding claim 30, Van Duuren et al. and Joo et al. together teach the method of claim 29. Van Duuren et al. further teaches forming protective spacers on sides of the conductive sidewall portions (**32** in Fig. 8), and wherein the implanting is in a region defined by the protective spacers (Fig. 8 shows the boundary of implant region **20** corresponding to the boundary of spacer **32**).

Response to Arguments

Applicant's arguments with respect to claims 27-30 have been considered but are moot in view of the new ground(s) of rejection.

Regarding claims 27-30, Applicant argues (p. 10, paragraphs 5 and 6) that Van Duuren et al. does not teach a plurality of strings of memory cells. Although Van Duuren et al. does not expressly teach this property of their invention, the device layout recited in claim 27 is not novel, as detailed above in the rejection.

Allowable Subject Matter

Claims 1-5, 8-18, 20-26, 31, and 33-36 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Claims 1-5, 8, 9, and 22-26 allowed for reasons given in the Office action dated 6/20/2005, namely that prior art does not teach or suggest, in combination with the other claimed limitations, wordlines that extend between floating gates into shallow trench isolation areas, thereby isolating adjacent floating gates, or T-shaped floating gates flanked by wordlines that are electrically coupled to isolating members between adjacent floating gates. Lee et al. (U.S. 2002/0028541) teaches T-shaped floating gates flanked by wordlines (Fig. 51), but the wordlines are not electrically coupled to the sidewall spacers between adjacent floating gates (a layer of dielectric separates the wordlines from the sidewall spacer, which itself is insulating). Furthermore, Lee et al. teaches a wordline that extends between floating gates, but into the source/drain regions, not into shallow trench isolation regions.

Prior art also does not teach or suggest shielding floating gates from adjacent floating gates that are diagonally or horizontally adjacent to the selected floating gate.

Finally, prior art does not teach or suggest forming a second set of parallel trenches in an oxide layer deposited within a first set of trenches and then forming wordlines that extend between adjacent floating gates into the second set of trenches.

Regarding claims 10-18, 35, and 36, prior art does not teach or suggest, in combination with the other claimed limitations, that the non-volatile storage device is a NAND flash memory. Van Duuren et al., the closest prior art of record, teaches a non-volatile floating gate semiconductor memory device, but does not teach that the device is a NAND flash memory.

Regarding claims 20 and 21, prior art does not teach or suggest, in combination with the other claimed limitations, that the means for reading the floating gates extends within means within the substrate for isolating adjacent floating gates.

Regarding claims 31 and 33-34, prior art does not teach or suggest, in combination with the other claimed limitations, a T-shaped floating gate. Van Duuren et al. does not teach floating gates with T-shaped cross sections, and there is no motivation to combine this reference with other relevant prior art.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO

Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

had

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